## CLAIMS

What is claimed is:

1. A stacked-chip semiconductor package, comprising:

a chip carrier having an upper surface and an opposite lower surface and formed with an opening penetrating therethrough;

a thermal blocking member applied at predetermined area on the upper surface of the chip carrier and over the opening, wherein the thermal blocking member has a first surface directed away from the opening and an opposite second surface facing toward the opening;

a first chip mounted on the first surface of the thermal blocking member and electrically connected to the upper surface of the chip carrier at area free of the thermal blocking member;

a second chip mounted on the second surface of the thermal blocking member and received within the opening of the chip carrier, allowing the second chip to be electrically connected to the lower surface of the chip carrier; and

an encapsulant for encapsulating the second chip and having a cavity for receiving and exposing the first chip.

2. The semiconductor package of claim 1, further comprising: a third chip stacked on the second chip and electrically connected to the lower surface of the chip carrier, allowing the third chip to be encapsulated by the encapsulant.
3. The semiconductor package of claim 1, further comprising: an infrared filter and a lens supported by the encapsulant, wherein the infrared filter is positioned above the first chip and the lens is disposed above the infrared filter, allowing light to penetrate through the lens and infrared filter to reach the first chip.
4. The semiconductor package of claim 1, wherein the first and second chips are electrically connected to the chip carrier by a plurality of bonding wires.
5. The semiconductor package of claim 2, wherein the third chip is electrically

connected to the chip carrier by a plurality of bonding wires.

6. The semiconductor package of claim 1, wherein the chip carrier is a substrate.
7. The semiconductor package of claim 1, wherein the chip carrier is a lead frame having a plurality of leads surrounding the opening.
8. The semiconductor package of claim 3, wherein the first chip is a CMOS (complementary metal oxide semiconductor) chip.
9. The semiconductor package of claim 1, wherein the thermal blocking member is made of a thermal resistant material.
10. A fabrication method of a stacked-chip semiconductor package, comprising the steps of:

preparing a chip carrier having an upper surface and an opposite lower surface, the chip carrier being formed with an opening penetrating therethrough;

applying a thermal blocking member at predetermined area on the upper surface of the chip carrier and over the opening, wherein the thermal blocking member has a first surface directed away from the opening and an opposite second surface facing toward the opening;

mounting a first chip on the first surface of the thermal blocking member and electrically connecting the first chip to the upper surface of the chip carrier at area free of the thermal blocking member;

mounting a second chip on the second surface of the thermal blocking member to be received within the opening of the chip carrier, and electrically connecting the second chip to the lower surface of the chip carrier; and

forming an encapsulant for encapsulating the second chip and having a cavity for receiving and exposing the first chip.

11. The fabrication method of claim 10, further comprising a step of: stacking a third chip on the second chip and electrically connecting the third chip to the lower surface of the chip carrier, allowing the third chip to be encapsulated by the

encapsulant.

12. The fabrication method of claim 10, further comprising a step of: mounting an infrared filter and a lens to be supported by the encapsulant, wherein the infrared filter is positioned above the first chip and the lens is disposed above the infrared filter, allowing light to penetrate through the lens and infrared filter to reach the first chip.
13. The fabrication method of claim 10, wherein the first and second chips are electrically connected to the chip carrier by a plurality of bonding wires.
14. The fabrication method of claim 10, wherein the third chip is electrically connected to the chip carrier by a plurality of bonding wires.
15. The fabrication method of claim 10, wherein the chip carrier is a substrate.
16. The fabrication method of claim 10, wherein the chip carrier is a lead frame having a plurality of leads surrounding the opening.
17. The fabrication method of claim 12, wherein the first chip is a CMOS (complementary metal oxide semiconductor) chip.
18. The fabrication method of claim 10, wherein the thermal blocking member is made of a thermal resistant material.